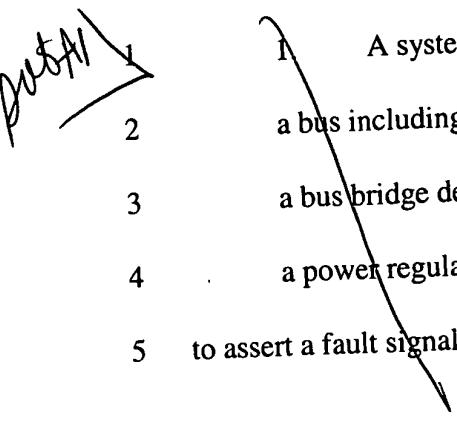
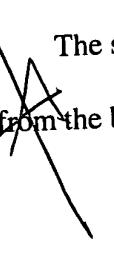


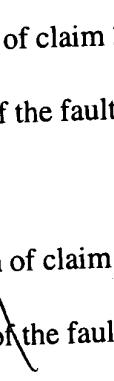
CLAIMS

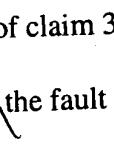
What is claimed is:

- put in* 
- 1 A system, comprising:
 - 2 a bus including a power line;
 - 3 a bus bridge device including an internal logic unit; and
 - 4 a power regulator to deliver power to the power line, the power regulator further
 - 5 to assert a fault signal to the bus bridge device if a power fault is detected.

- sub 1* 
- 1 2. The system of claim 1, the bus bridge device to disconnect the internal
 - 2 logic unit from the bus in response to an assertion of the fault signal.

- sub 2* 
- 1 3. The system of claim 2, the power regulator to cease to deliver power to the
 - 2 power line if a power fault is detected.

- sub 3* 
- 1 4. The system of claim 3, the bus bridge device to assert an interrupt signal in
 - 2 response to the assertion of the fault signal.

- sub 4* 
- 1 5. The system of claim 3, the bus bridge device to assert an error signal in
 - 2 response to the assertion of the fault signal.

DRAFT 1

6. The system of claim 3, the bus bridge device to assert a power enable
2 signal to the power regulator upon system startup, the power regulator to deliver power to
3 the power line in response to the assertion of the power enable signal.

1 7. The system of claim 6, the bus bridge device to deassert the power enable
2 signal follow the assertion of the fault signal.

1 8. The system of claim 7, the power regulator module to deassert the fault
2 signal in response to the deassertion of the power enable signal.

1 9. The system of claim 8, wherein the bus is a PCI bus.

1 10. A bus bridge device, comprising:
2 a bus interface unit coupled to bus bridge device to a bus;
3 an internal logic unit coupled to the bus interface unit; and
4 a fault signal input, the bus bridge device to disconnect the internal logic unit
5 from the bus in response to an assertion of the fault signal.

1 11. The bus bridge device of claim 10, further comprising an interrupt signal
2 output, the bus bridge device to assert the interrupt signal output in response to the
3 assertion of the fault signal.

sub A1

1 12. The bus bridge device of claim 10, further comprising an error signal
2 output, the bus bridge device to assert the error signal in response to the assertion of the
3 fault signal.

1 13. A method, comprising:
2 applying power to a bus;
3 detecting a power fault;
4 removing power from the bus; and
5 asserting a fault signal to a bus bridge device.

1 14. The method of claim 13, further comprising the bus bridge device
2 disconnecting an internal logic unit from the bus in response to the assertion of the fault
3 signal.

1 15. The method of claim 14, further comprising asserting an interrupt signal
in response to the assertion of the fault signal.

1 16. The method of claim 14, further comprising asserting an error signal in
2 response to the assertion of the fault signal.